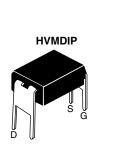


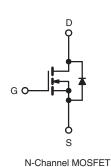
Vishay Siliconix

COMPLIANT

## **Power MOSFET**

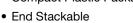
PRODUCT SUMMARY				
V <sub>DS</sub> (V)	60			
$R_{DS(on)}(\Omega)$	$V_{GS} = 10 \text{ V}$	0.8		
Q <sub>g</sub> (Max.) (nC)	7			
Q <sub>gs</sub> (nC)	2			
Q <sub>gd</sub> (nC)	7			
Configuration	Single			





#### **FEATURES**

- For Automatic Insertion
- Compact Plastic Package



- Fast Switching
- Low Drive Current
- · Easily Paralleled
- Excellent Temperature Stability
- Compliant to RoHS Directive 2002/95/EC

#### Note

\* Pb containing terminations are not RoHS compliant, exemptions may apply

#### **DESCRIPTION**

The HVMDIP technology is the key to Vishay's advanced line of power MOSFET transistors. The efficient geometry and unique processing of the HVMDIP design achieves very low on-state resistance combined with high transconductance and extreme device ruggedness. HVMDIPs feature all of the established advantages of MOSFETs such as voltage control, very fast switching, ease of paralleling, and temperature stability of the electrical parameters.

The HVMDIP 4 pin, dual-in-line package brings the advantages of HVMDIPs to high volume applications where automatic PC board insertion is desireable, such as circuit boards for computers, printers, telecommunications equipment, and consumer products. Their compatibility with automatic insertion equipment, low-profile and end stackable features represent the stat-of-the-art in power device packaging.

ORDERING INFORMATION	
Package	HVMDIP
Lead (Pb)-free	IRFD113PbF
	SiHFD113-E3

<b>ABSOLUTE MAXIMUM RATINGS</b> (T <sub>C</sub> = 25 °C, unless otherwise noted)							
PARAMETER			SYMBOL	LIMIT	UNIT		
Drain-Source Voltage <sup>a</sup>			$V_{DS}$	60	V		
Gate-Source Voltage			$V_{GS}$	± 20			
Continuous Drain Current	V <sub>GS</sub> at 10 V	T <sub>C</sub> = 25 °C	I <sub>D</sub>	0.8	^		
Pulsed Drain Current <sup>b</sup>			I <sub>DM</sub>	6.4	Α		
Linear Derating Factor				0.008	W/°C		
Inductive Current, Clamped	L = 100 μH		I <sub>LM</sub>	6.4	Α		
Maximum Power Dissipation	T <sub>C</sub> = 25 °C		$P_{D}$	1.0	W		
Operating Junction and Storage Temperature Range		T <sub>J</sub> , T <sub>stg</sub>	- 55 to + 150	°C			
Soldering Recommendations (Peak Temperature)	for 10 s			300c	1		

#### Notes

- a.  $T_J = 25$  °C to 150 °C
- b. Repetitive rating; pulse width limited by maximum junction temperature.
- c. 1.6 mm from case.



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THERMAL RESISTANCE RATINGS					
PARAMETER	SYMBOL TYP.		MAX.	UNIT	
Maximum Junction-to-Ambient	R <sub>thJA</sub>	-	120	°C/W	

PARAMETER	SYMBOL	TES	TEST CONDITIONS			MAX.	UNIT		
Static									
Drain-Source Breakdown Voltage	V <sub>DS</sub>	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$		60	-	-	.,		
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =	· V <sub>GS</sub> , I <sub>D</sub> = 250 μA	2.0	-	4.0	V		
Gate-Source Leakage	I <sub>GSS</sub>	,	V <sub>GS</sub> = ± 20 V	-	-	± 500	nA		
Zero Gate Voltage Drain Current	1	$V_{DS} = m$	$V_{DS}$ = max. rating, $V_{GS}$ = 0 V $V_{DS}$ = max. rating x 0.8, $V_{GS}$ = 0 V, $V_{CS}$ = 125 °C		$V_{DS}$ = max. rating, $V_{GS}$ = 0 V		-	250	
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = max. rating			-	1000	μA		
On-State Drain Current <sup>b</sup>	I <sub>D(on)</sub>	V <sub>GS</sub> = 10 V	$V_{DS} > I_{D(on)} \times R_{DS(on)} \max$ .	0.8	-	-	Α		
Drain-Source On-State Resistance <sup>b</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 0.8 A	-	0.6	0.8	Ω		
Forward Transconductanceb	9 <sub>fs</sub>	$V_{DS} > I_{D(on)}$	$V_{DS} > I_{D(on)} \times R_{DS(on)} \text{ max., } I_D = 0.8 \text{ A}$		1.2	-	S		
Dynamic									
Input Capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0 V,		-	135	200	pF		
Output Capacitance	C <sub>oss</sub>		$V_{DS} = 25 \text{ V},$		80	100			
Reverse Transfer Capacitance	C <sub>rss</sub>	f = 1.0 MHz		-	20	25			
Total Gate Charge	Qg			1	5	7			
Gate-Source Charge	Q <sub>gs</sub>	V <sub>GS</sub> = 10 V	$V_{GS} = 10 \text{ V}$ $V_{DS} = 0.8 \text{ max. rating}$		2	-	nC		
Gate-Drain Charge	Q <sub>gd</sub>				7	-			
Turn-On Delay Time	t <sub>d(on)</sub>				10	20	- ns		
Rise Time	t <sub>r</sub>	$V_{DD} = 0.5 V_{DS}$ , $I_D = 0.8 A$ , $R_g = 50 \Omega$		1	15	25			
Turn-Off Delay Time	t <sub>d(off)</sub>			-	15	25			
Fall Time	t <sub>f</sub>			-	10	20			
Internal Drain Inductance	L <sub>D</sub>	Between lead, 2 mm (0.08") from package and center of die contact		-	4.0	-			
Internal Source Inductance	L <sub>S</sub>			-	6.0	-	nH		
Drain-Source Body Diode Characteristic	s								
Continuous Source-Drain Diode Current	I <sub>S</sub>		MOSFET symbol		-	0.8			
Pulsed Diode Forward Current	I <sub>SM</sub>	showing the integral reverse p - n junction diode		-	-	6.4	A		
Body Diode Voltage <sup>a</sup>	V <sub>SD</sub>	T <sub>A</sub> = 25 °C, I <sub>S</sub> = 0.8 A, V <sub>GS</sub> = 0 V		-	-	2	V		
Body Diode Reverse Recovery Time	t <sub>rr</sub>	- T <sub>J</sub> = 150 °C, I <sub>F</sub> = 1.0 A, dl/dt = 100 A/μs		1	100	-	ns		
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>			-	0.2	-	μC		
Forward Turn-On Time	t <sub>on</sub>	Intrinsic turn-on time is negligible (turn-on is dominated by L <sub>S</sub> and L <sub>D</sub> )				_D)			

#### Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).

b. Pulse width  $\leq 300~\mu s;$  duty cycle  $\leq 2~\%.$ 



### TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

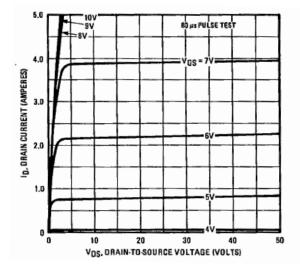


Fig. 1 - Typical Output Characteristics

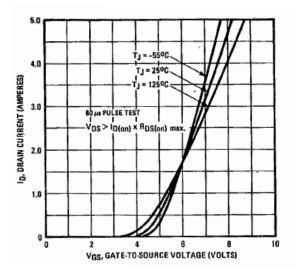


Fig. 2 - Typical Transfer Characteristics

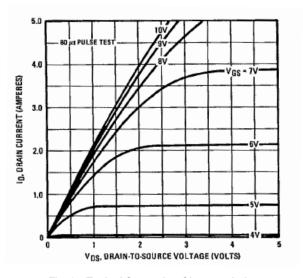


Fig. 3 - Typical Saturation Characteristics

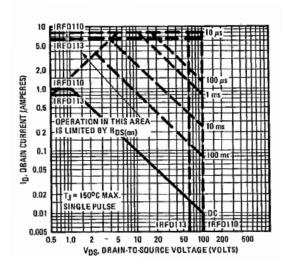


Fig. 4 - Maximum Safe Operatung Area



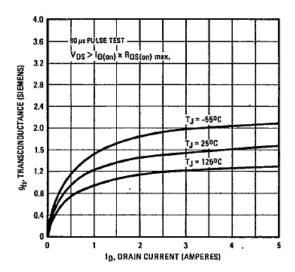


Fig. 5 - Typical Transconductance vs. Drain Current

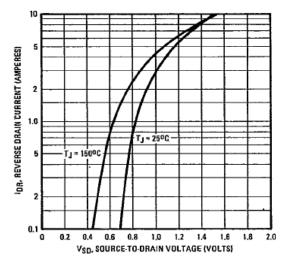


Fig. 6 - Typical Source-Drain Diode Forward Voltage

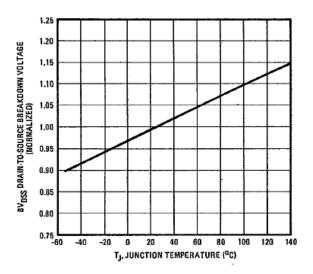


Fig. 7 - Breakdown Voltage vs. Temperature

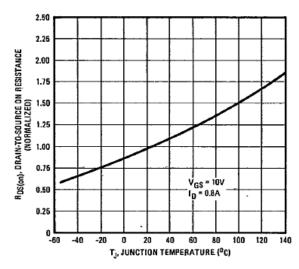


Fig. 8 - Normalized On-Resistance vs. Temperature



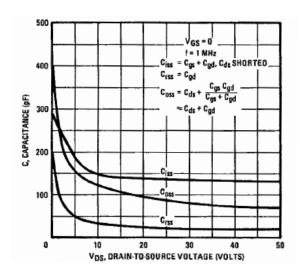


Fig. 9 - Typical Capacitance vs. Drain-to-Source Voltage

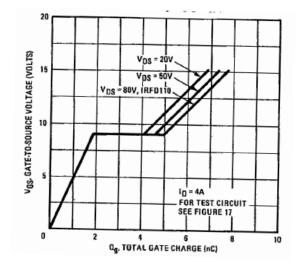


Fig. 10 - Typical Gate Charge vs. Gate-to-Source Voltage

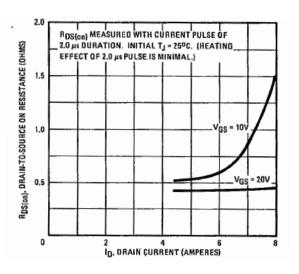


Fig. 11 - Typical On-Resistance vs. Darin Current

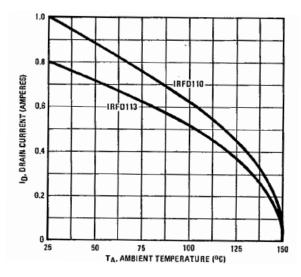


Fig. 12 - Maximum Darin Current vs. Case Temperature



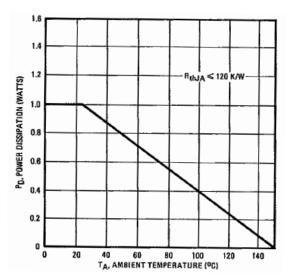


Fig. 13 - Power vs. Temperature Derating

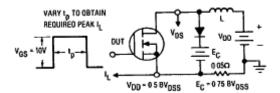


Fig. 14 - Clamped Inductive Test Circuit

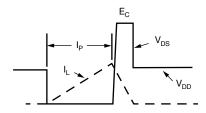


Fig. 15 - Clamped Inductive Waveforms

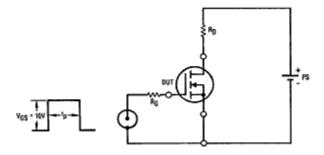


Fig. 16 - Switching Time Test Circuit

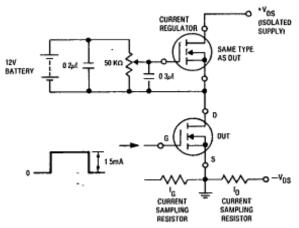


Fig. 17 - Gate Charge Test Circuit

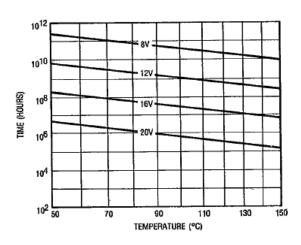


Fig. 18 - Typical Time to Accumulated 1 % Gate Failure

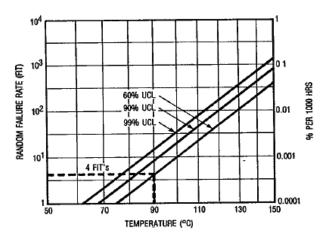
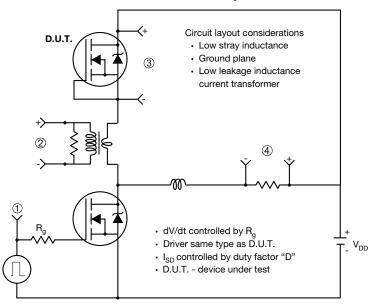


Fig. 19 - Typical High Temperature Reverse Bias (HTRB) Failure Rate



#### Peak Diode Recovery dV/dt Test Circuit



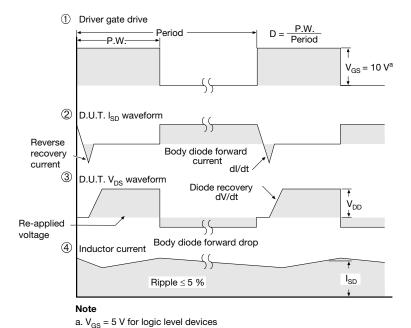


Fig. 20 - For N-Channel

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